

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A single track-and-hold circuit having an input signal (V_{in}) and an output signal (V_s), a bootstrap switch (14a) having as its inputs a clock signal and an input signal (v_{in}), said input signal (v_{in}) of said bootstrap switch (14a) being connected to said output signal (V_s) of said circuit via a current source (20) and a buffering transistor (30), characterized in that said input signal (v_{in}) of said bootstrap switch (14a) comprises said output signal (V_s) of said circuit; said single track-and-hold circuit further comprising a capacitor (12), said input signal (V_{in}) being connected to said capacitor (12) via a switch (10), said switch (10) being closed during a track mode of said circuit and open during a hold mode of said circuit, said bootstrap switch (14a) having as an output to said switch (10), a clock signal ($clkboot$) equal to said input signal (V_{in}) added to a supply voltage (V_{dd}); and

including a second bootstrap switch (14b), the input signal (v_{in}) of which is connected to said output signal (V_s) of said single track-and-hold circuit via said current source (20) and said buffering transistor (30) of said single track-and-hold circuit.

2. (canceled)

3. (previously presented) A single track-and-hold circuit according to claim 1, wherein said buffering transistor (30) comprises a MOS transistor.

4. (previously presented) A single track-and-hold circuit according to claim 3, wherein said MOS transistor (30) is a PMOS transistor.

5. (canceled)

6. (previously presented) A single track-and-hold circuit according to claim 1, further comprising one or more dummy switches (16) which are clocked in anti-phase to said switch (10) connecting said input signal (Vin) to said capacitor (12).

7. (previously presented) A single track-and-hold circuit according to claim 6, wherein said input signal (Vin) is connected to said dummy switches (16) via said second bootstrap switch (14b), having as an additional input an anti-phase clock signal.

8. (original) An analog-to-digital converter including a track-and-hold circuit according to claim 1.

9. (original) An integrated circuit including an analog-to-digital converter according to claim 8.